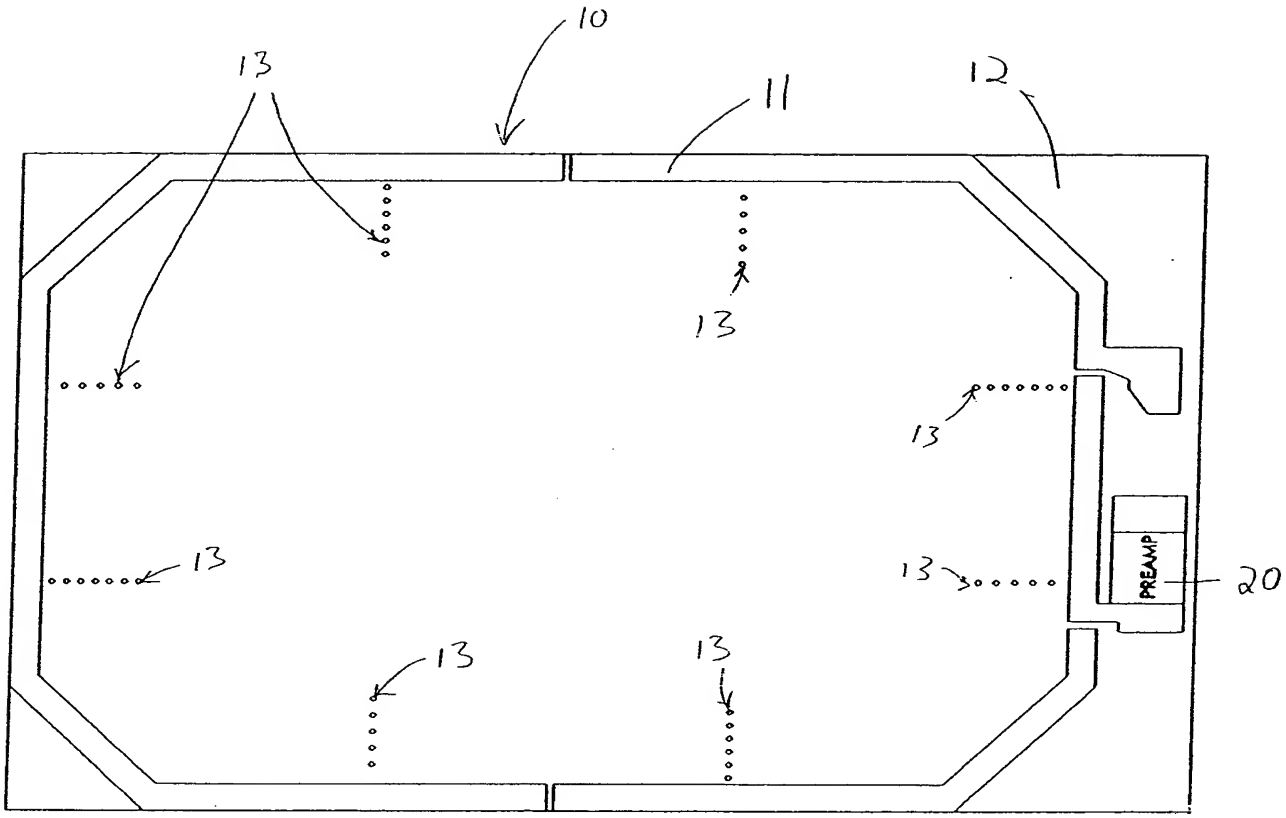

Fig. 1

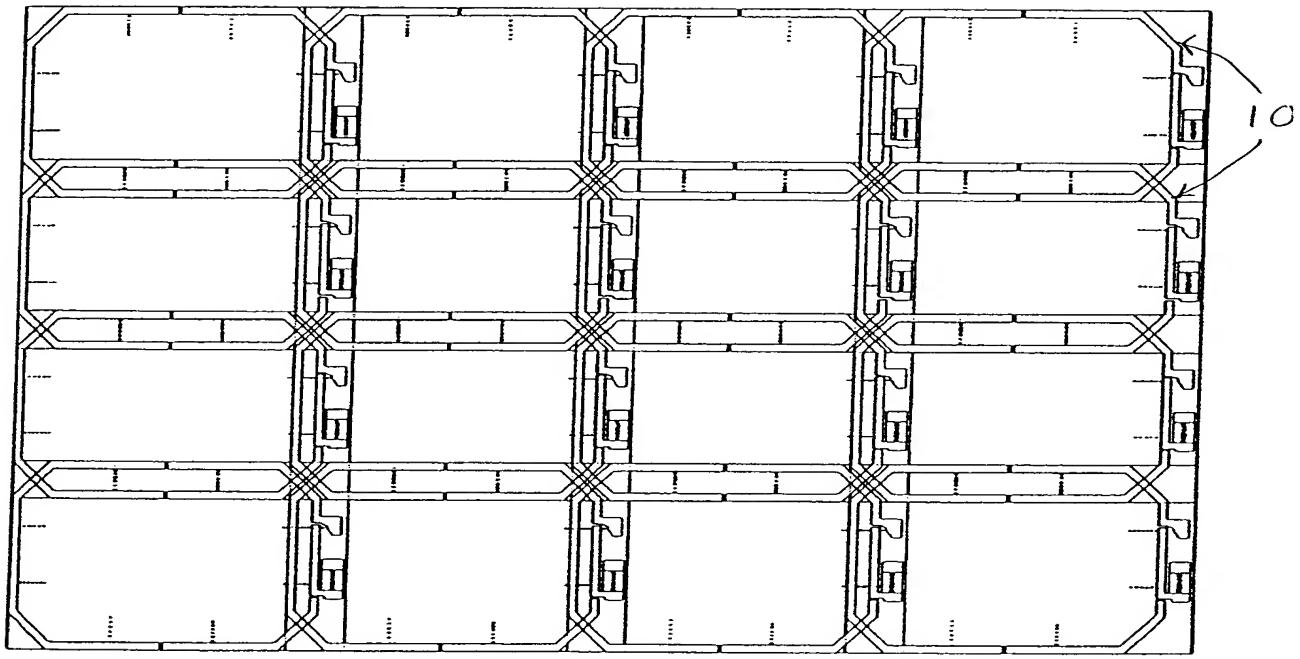

Fig. 2

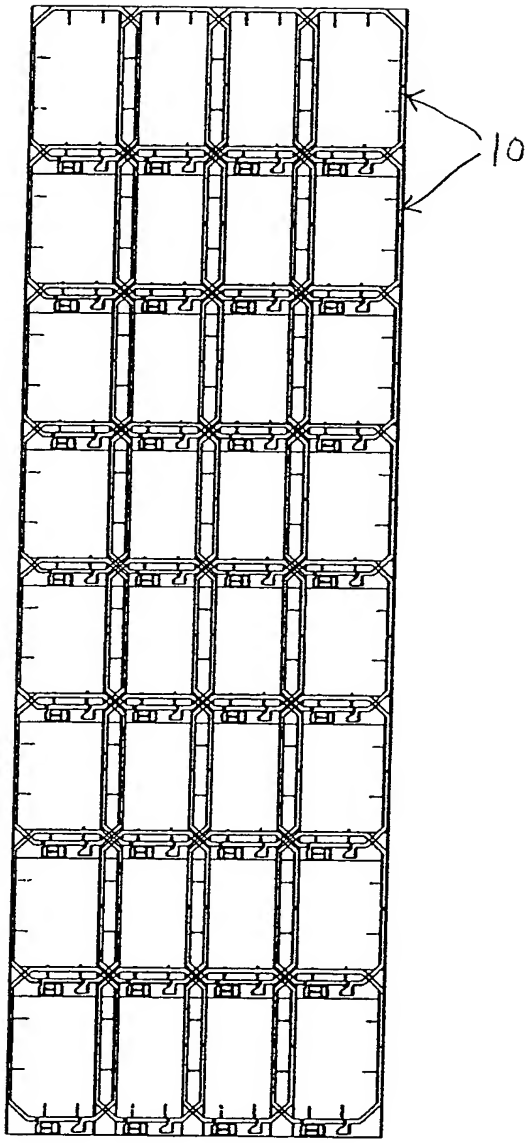

Fig. 3

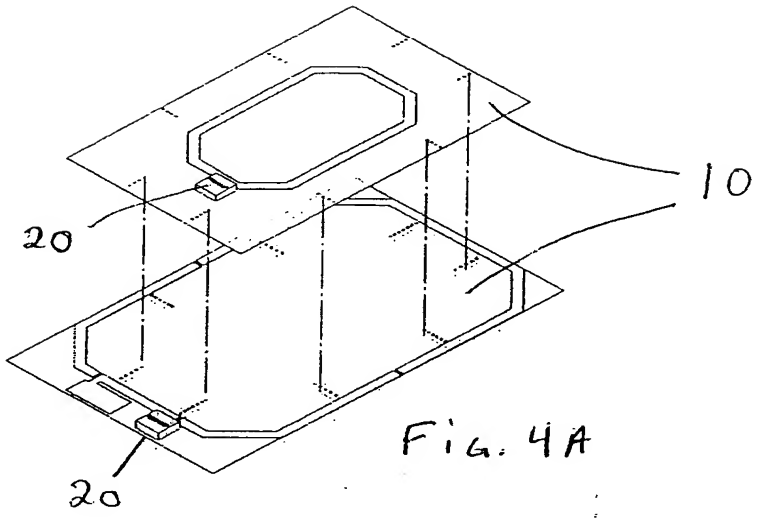

Fig. 4A

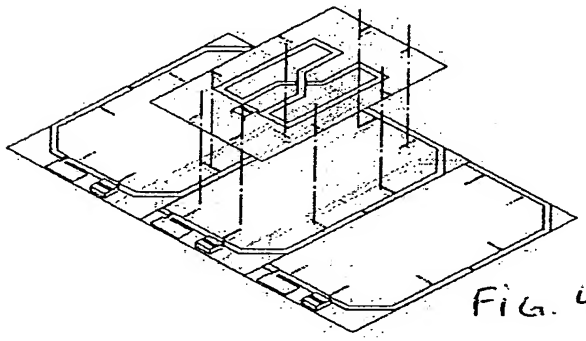

Fig. 4B

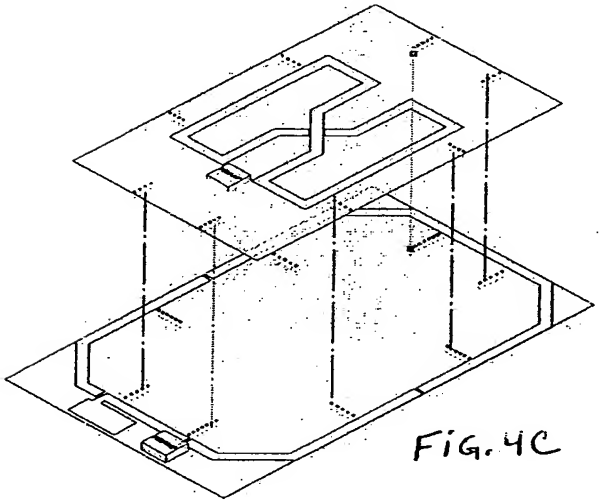

Fig. 4C

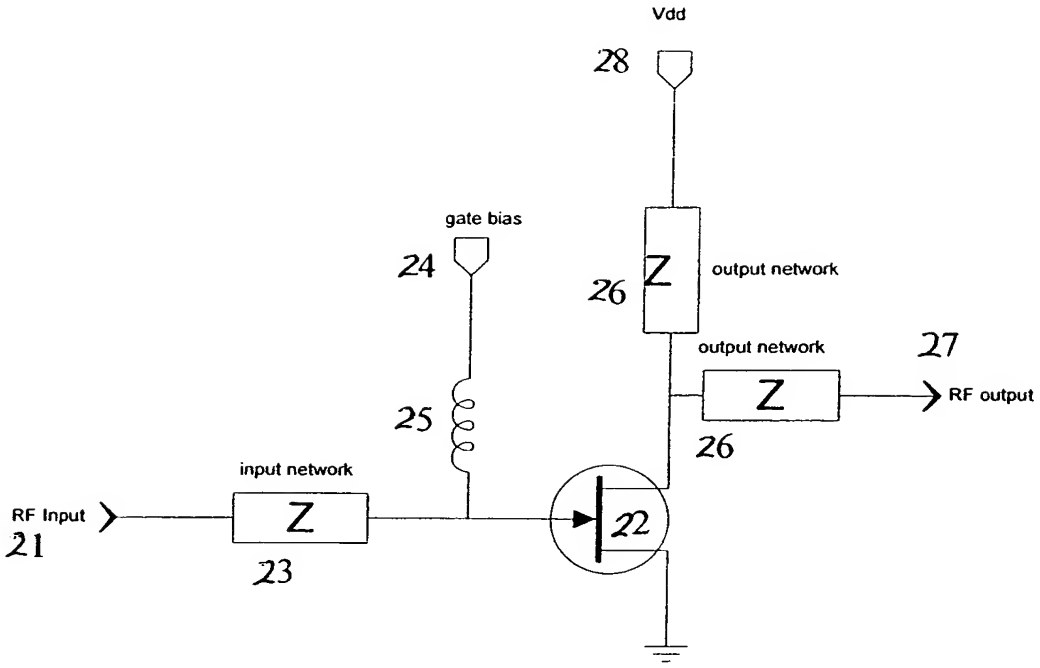
Vdd
28
gate bias
24
Z
26
output network
output network
27
Z
RF output
26
25
input network
RF Input
21
Z
23
22

Fig. 5